Central tracker for BM@N experiment based on double side Si- microstrip detectors

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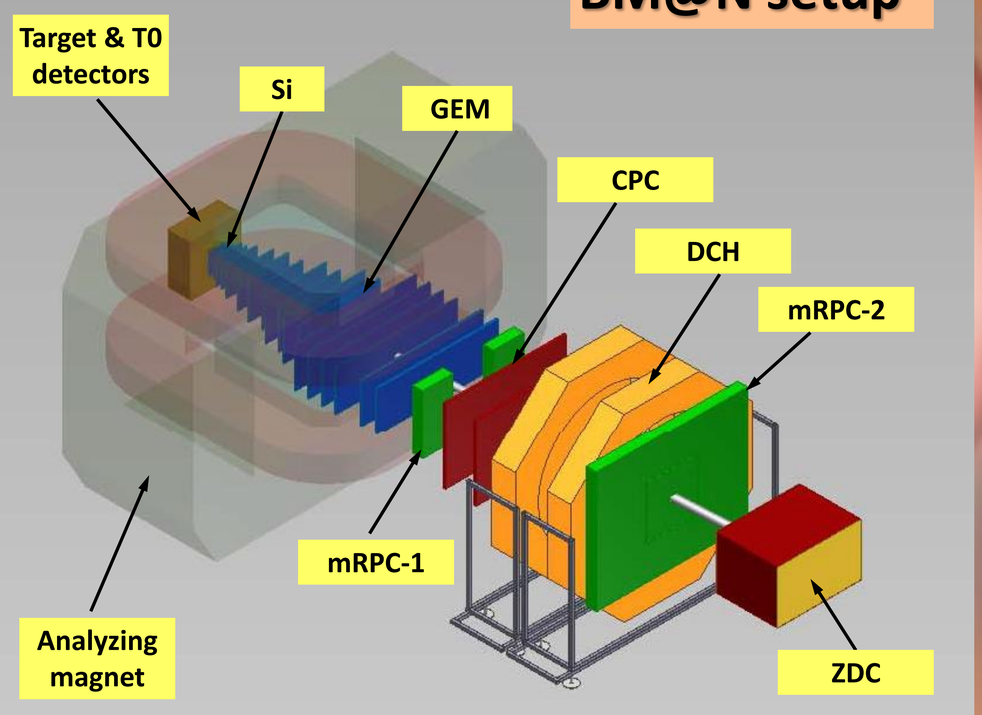
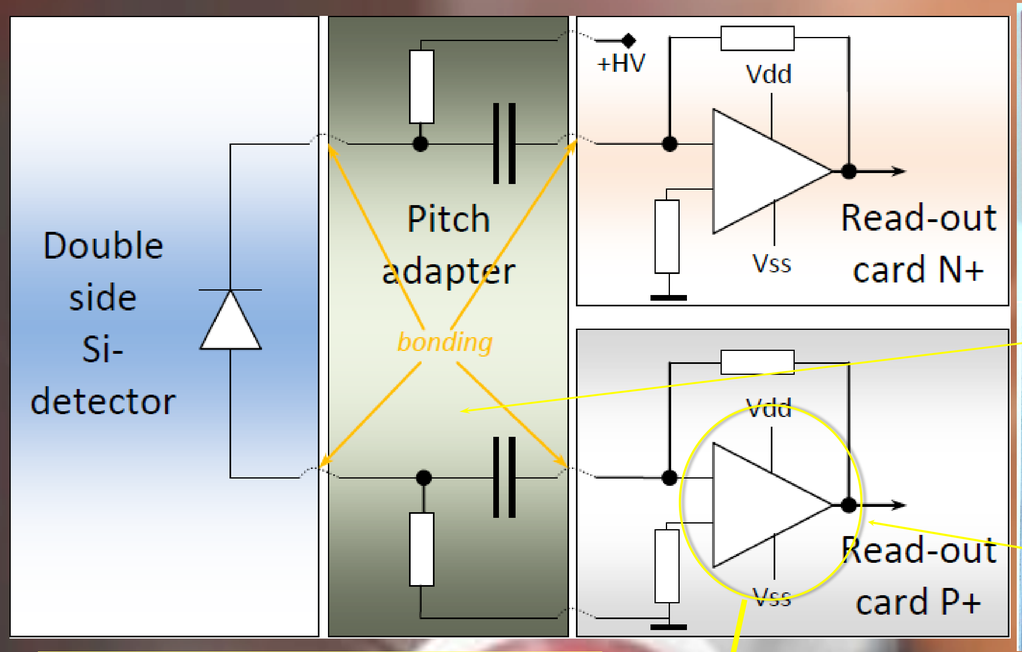
BM@N setup

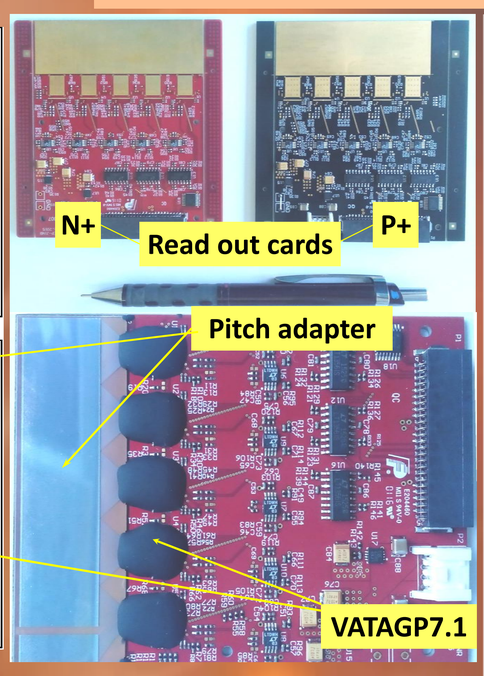


- Central tracker (GEM + Si) inside analyzing magnet to reconstruct AA interaction
- Outer tracer (DCH, CPC) behind magnet to link central tracks to ToF detectors
- ToF system based on mRPC and T0 detectors to identify hadrons and light nucleus
- ZDC calorimeter to measure centrality of AA collisions and trigger generation
- Detectors to generation T0, trigger L1 centrality and beam monitoring
- Electromagnetic calorimeter - for γ, e+ e- identification

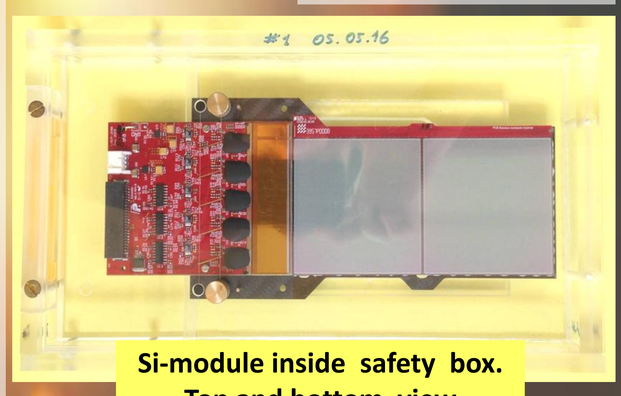
- 2-coordinate Si detector X-X'(±2.5°) with pitch of 95/103μm, full size 250x250 mm
- Each module consists of 2 double side Silicon detectors (DSSD) detectors of 300μm thickness and size 63x63 mm
- Total number of read out channels – 10240
- One plane is installed in front of GEM tracker in the February 2017

1280ch Si-module

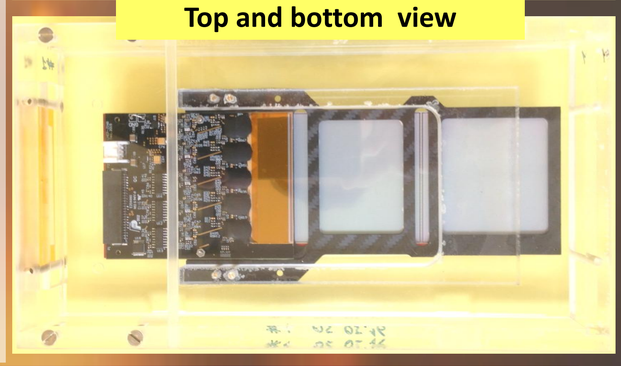




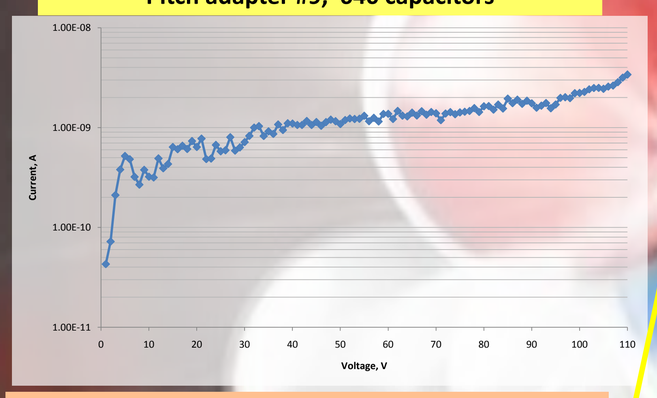
- Read-out electronics based on VATAGP7.1 ASICs from IDEAS company
- Each read-out card combined of 5 ASICs which give 640 read-out channels
- Each Si-module has two read-out cards. One is for N+ side of DSSD and other is for P+ side
- Special pitch adapter (SOI- poly silicon resistors 2 MOhm and integrated capacitors 150pF x 150V) on sapphire substrate have been designed for direct connection detector to read-out card

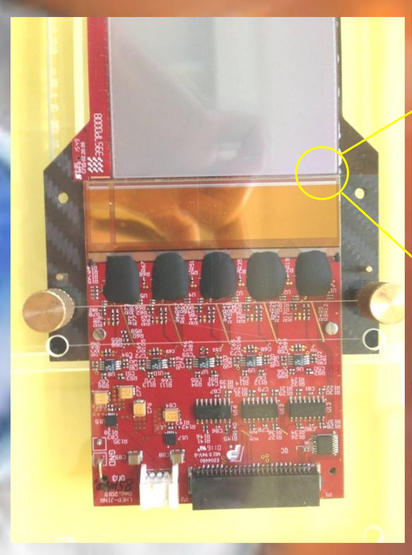


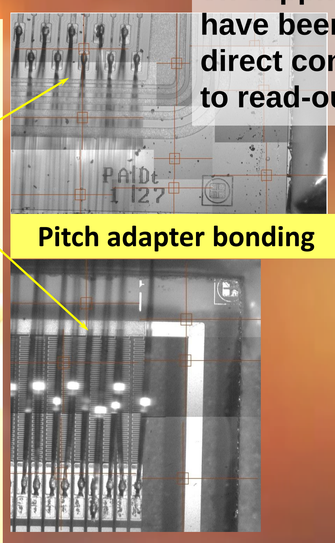
Si-module inside safety box. Top and bottom view



Total capacitors leakage current vs HV voltage. Pitch adapter #9, 640 capacitors

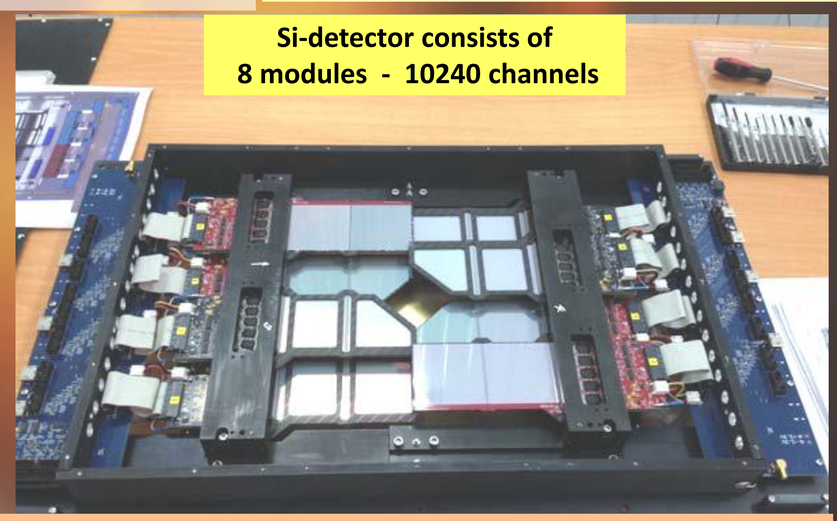






Pitch adapter bonding

Si-detector consists of 8 modules - 10240 channels



Readout electronics

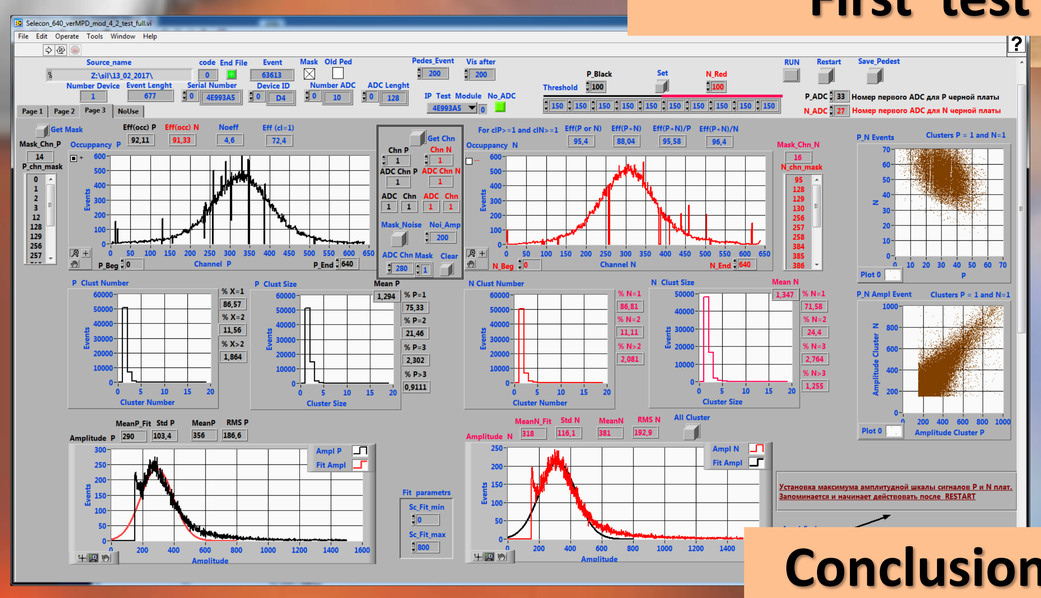
The VATAGP7.1 is a 128-channel charge sensitive amplifier. Each channel features low-noise/low power buffered preamplifiers, shaper with sample/hold, multiplexed analogue readout. In addition, each channel has a fast shaper that gives a trigger signal.

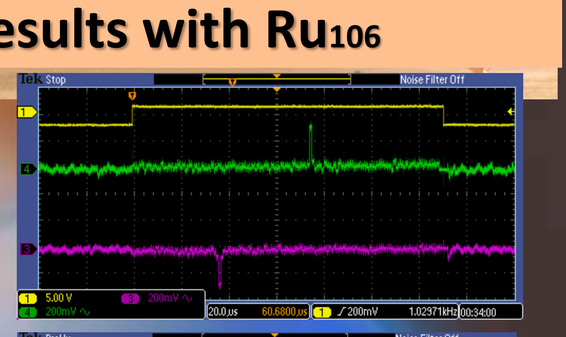
Analog specification:

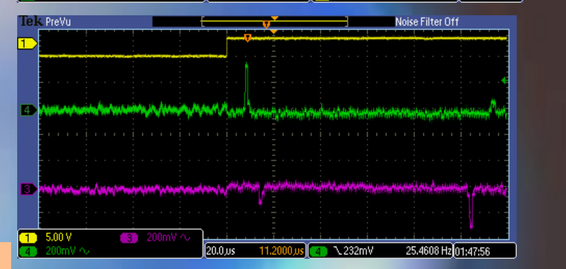
- 128 input analog channels
- Gain – 16.5μA/fC
- Dynamic range ±30fC
- Peaking time (slow shaper) – 500ns typically
- Peaking time (fast shaper) – 50 ns typically
- Electronic noise (zero input capacitance) – 70 e^-
- Electronic noise, slope – 12e^-/pF

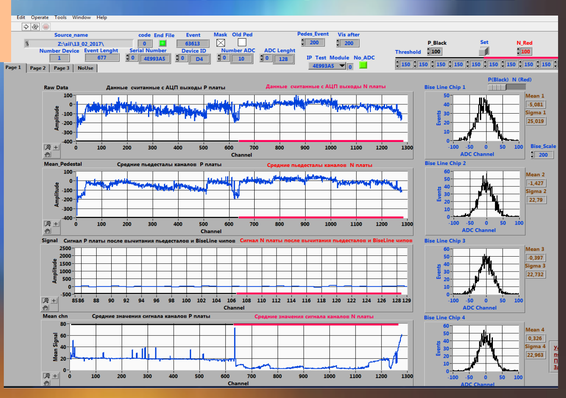
VATAGP7.1 has three different readout modes : serial readout, sparse readout and sparse readout with neighbor channels.

First test results with Ru_{106}









Thanks for help

Our group is very grateful to the following companies for its help in creation of Si-detector: RIMST (Zelenograd)- for design and creation of sensor and pitch adapter, MELT – for ASICs bonding and capsulation, IDEAS – for providing consultations for ASICs operation.

Conclusion

- *Si-detector was invented, designed and assembled in LHEP JINR.*
- *Si-detector was built on DC-coupling technology that simplifier sensor and made it more reliable*
- *All accessories were produced in Russia or provided by commercially company (IDEAS)*
- *Si-detector is installed into the BM@N setup as a part the central tracker*